18-Bit, 2 MSPS SAR ADC

Preliminary Technical Data

AD7641

FEATURES

Throughput:
- **2 MSPS (Warp mode)**
- **1.5 MSPS (Normal mode)**

18-bit resolution with no missing codes
2.048V internal low drift refernce
INL: ±2 LSB typical
S/(N+D): 93 dB typical @ 20 kHz
THD: −115 dB typical @ 20 kHz
Differential input range: ±V_{REF} (V_{REF} up to 2.5 V)
No pipeline delay (SAR architecture)
Parallel (18-, 16-, or 8-bit bus)
Serial 5 V/3.3 V/2.5 V interface
SPI®/QSPI™/MICROWIRE™/DSP compatible
Single 2.5 V supply operation
Power dissipation: 65 mW typical @ 2 MSPS
Power-down mode
48-LQFP and LFCSP packages
Speed upgrade of the AD7674

APPLICATIONS

Medical instruments
High dynamic data acquisition
Instrumentation
Spectrum analysis
ATE

FUNCTIONAL BLOCK DIAGRAM

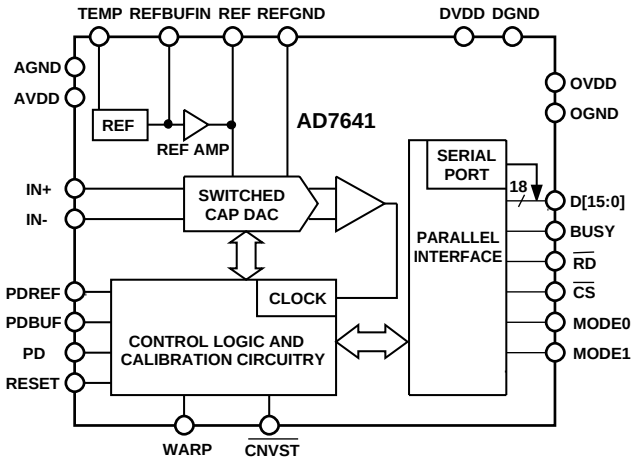

Figure 1.

Table 1. PulSAR Selection

	kSPS			
Type	**100 to 250**	**500 to 570**	**800 to 1000**	**>1000**
Pseudo Differential	AD7651 AD7660/61	AD7650/52 AD7664/66	AD7653 AD7667	
True Bipolar	AD7663	AD7665	AD7671	
True Differential	AD7675	AD7676	AD7677	AD7621
18 Bit	AD7678	AD7679	AD7674	AD7641
Multichannel/ Simultaneous		AD7654	AD7655	

GENERAL DESCRIPTION

The AD7641 is a 18-bit, 2 MSPS, charge redistribution SAR, fully differential, analog-to-digital converter that operates from a single 2.5 V power supply. The part contains a high-speed 18-bit sampling ADC, an internal conversion clock, an internal reference and buffer, error correction circuits, and both serial and parallel system interface ports. It features a very high sampling rate mode (Warp) and a fast mode (Normal) for asynchronous conversion rate applications. The AD7641 is hardware factory calibrated and comprehensively tested to ensure ac parameters such as signal-to-noise ratio (SNR) and total harmonic distortion (THD) in addition to the more traditional dc parameters of gain, offset and linearity. Operation is specified from −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. High Resolution and Fast Throughput.
   The AD7641 is a 2 MSPS, charge redistribution, 18-bit SAR ADC (no latency).
2. Superior INL.
   The AD7641 has a typical integral nonlinearity of 2 LSB with no missing 18-bit codes.
3. Internal Reference
   The AD7641 has a 2.048V, low drift, internal reference.
4. Single-Supply Operation.
   Operates from a single 2.5 V supply. Also features a power-down mode.
5. Serial or Parallel Interface.
   Versatile parallel (18-, 16-, or 8-bit bus) or 2-wire serial interface arrangement compatible with either 2.5 V, 3.3 V, or 5 V logic.

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Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		18			Bits
ANALOG INPUT					
Voltage Range	$V_{IN+} - V_{IN-}$	$-V_{REF}$		V_{REF}	V
Operating Input Voltage	V_{IN+}, V_{IN-} to AGND	–0.1		AVDD[1]	V
Analog Input CMRR	f_{IN} = 100 kHz		55		dB
Input Current	2 MSPS Throughput		50		µA
Input Impedance[2]					
THROUGHPUT SPEED					
Complete Cycle	In Warp Mode			500	ns
Throughput Rate	In Warp Mode	0.001		2	MSPS
Time between Conversions	In Warp Mode			1	ms
Complete Cycle	In Normal Mode			667	ns
Throughput Rate	In Normal Mode	0		1.5	MSPS
DC ACCURACY					
Integral Linearity Error		-3	±2	+3	LSB[3]
No Missing Codes		18			Bits
Differential Linearity Error		-1		+TBD	LSB
Transition Noise	V_{REF} = 2.5V		33		μV_{RMS}
Zero Error, T_{MIN} to T_{MAX}[4]			±30		LSB
Zero Error Temperature Drift			±1.0		ppm/°C
Gain Error, T_{MIN} to T_{MAX}[4]			±0.04		% of FSR
Gain Error Temperature Drift			±1.0		ppm/°C
Power Supply Sensitivity	AVDD = 2.5 V ± 5%		±3		LSB
AC ACCURACY					
Dynamic Range	V_{REF} = 2.5V		94.5		dB[5]
Signal-to-Noise	f_{IN} = 20kHz, V_{REF} = AVDD		93.5		dB
	f_{IN} = 20kHz, V_{REF} = 2.048		92.1		dB
Spurious Free Dynamic Range	f_{IN} = 20 kHz		110		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		–115		dB
Signal-to-(Noise + Distortion)	f_{IN} = 20 kHz		93		dB
–3 dB Input Bandwidth			50		MHz
SAMPLING DYNAMICS					
Aperture Delay			1		ns
Aperture Jitter			5		ps rms
Transient Response	Full-Scale Step			160	ns
INTERNAL REFERENCE	PDREF = PDBUF = LOW				
Output Voltage	@ 25°C		2.048		V
Output Voltage Hysteresis	–40°C to +85°C		50		ppm
Temperature Drift	–40°C to +85°C		±3		ppm/°C
Long-Term Drift			100		ppm/1000 Hours
Line Regulation	AVDD = 2.5 V ± 5%		±15		ppm/V
Turn-On Settling Time	C_{REF} = 10 µF		5		ms
Bandgap (REFBUFIN) Output Voltage			1.207		V
Bandgap (REFBUFIN) Output Resistance			6.33		kΩ
EXTERNAL REFERENCE	PDREF = PDBUF = HIGH				
Voltage Range		1.8	2.048	AVDD + 0.1	V
Current Drain	2 MSPS Throughput		TBD		µA
REFERENCE BUFFER	PDREF = HIGH, PDBUF = LOW				
Input Voltage Range (REFBUFIN)		1.05	1.2	1.52	V

Parameter	Conditions	Min	Typ	Max	Unit
TEMPERATURE PIN	@ 25°C				
Voltage Output			300		mV
Temperature Sensitivity			1		mV/°C
Output Resistance			4.7		kΩ
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.6	V
V_{IH}		1.7		5.25	V
I_{IL}		–1		+1	µA
I_{IH}		–1		+1	µA
DIGITAL OUTPUTS					
Data Format[6]					
Pipeline Delay[7]					
V_{OL}	I_{SINK} = 500 µA			0.4	V
V_{OH}	I_{SOURCE} = –500 µA	OVDD – 0.3			V
POWER SUPPLIES					
Specified Performance					
AVDD		2.37	2.5	2.63	V
DVDD		2.37	2.5	2.63	V
OVDD		2.30		3.6	V
Operating Current[8]	2 MSPS Throughput				
AVDD[9]	With Internal Reference		21.4		mA
DVDD[10]			2.7		mA
OVDD			1.4		mA
Power Dissipation[8, 9]	2 MSPS Throughput				
With Internal Reference			65		mW
Without Internal Reference			58		mW
In Power-Down Mode	PD = HIGH		TBD		µW
TEMPERATURE RANGE[11]					
Specified Performance	T_{MIN} to T_{MAX}	–40		+85	°C

[1] When using an external reference. With the internal reference, the input range is from -0.1V to V_{REF}.
[2]See Analog Inputs section.
[3]LSB means least significant bit. With the ±2.048 V input range, 1 LSB is 15.63 µV.
[4]See Voltage Reference Input section. These specifications do not include the error contribution from the external reference.
[5]All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale, unless otherwise specified.
[6]Parallel or serial 16-bit.
[7]Conversion results are available immediately after completed conversion.
[8] In Warp mode.
[9] With REF, PDREF and PDBUF are LOW; without REF, PDREF and PDBUF are HIGH.
[10] Tested in parallel reading mode.
[11]Consult factory for extended temperature range.

TIMING SPECIFICATIONS

Table 3. AVDD = DVDD = 2.5V; OVDD = 2.3V to 3.6V; V_{REF} = 2.5V; all specifications T_{MIN} to T_{MAX} unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
Refer to Figure 33 and Figure 34					
Convert Pulse Width	t_1	5			ns
Time Between Conversions (Warp Mode/Normal Mode)[1]	t_2	500/667			ns
$\overline{CNVST}$ low to BUSY high Delay	t_3			30	ns
BUSY high All Modes Except in Master Serial Read After Convert (Warp Mode/Normal Mode)	t_4			400/520	ns
Aperture Delay	t_5		1		ns
End of Conversion to BUSY low Delay	t_6	10			ns
Conversion Time (Warp Mode/Normal Mode)	t_7			400/520	ns
Acquisition Time (Warp Mode/Normal Mode)	t_8	100/147			ns
RESET Pulsewidth	t_9	10			ns
Refer to Figure 35, Figure 36, and Figure 37(Parallel Interface Modes)					
$\overline{CNVST}$ low to Data Valid Delay (Warp Mode/Normal Mode)	t_{10}			400/520	ns
Data Valid to BUSY low Delay	t_{11}	20			ns
Bus Access Request to Data Valid	t_{12}			40	ns
Bus Relinquish Time	t_{13}	2		17	ns
Refer to and Figure 39 and Figure 40					
$\overline{CS}$ low to SYNC Valid Delay	t_{14}			10	ns
$\overline{CS}$ low to Internal SCLK Valid Delay	t_{15}			10	ns
$\overline{CS}$ low to SDOUT Delay	t_{16}			10	ns
$\overline{CNVST}$ low to SYNC Delay (Warp Mode/Normal Mode)	t_{17}		12/137		ns
SYNC Asserted to SCLK First Edge Delay [2]	t_{18}	3			ns
Internal SCLK Period [2]	t_{19}	12		40	ns
Internal SCLK high [2]	t_{20}	4			ns
Internal SCLK low [2]	t_{21}	4			ns
SDOUT Valid Setup Time	t_{22}	2			ns
SDOUT Valid Hold Time	t_{23}	1			ns
SCLK Last Edge to SYNC Delay [2]	t_{24}	0			ns
$\overline{CS}$ high to SYNC HI-Z	t_{25}			10	ns
$\overline{CS}$ high to Internal SCLK HI-Z	t_{26}			10	ns
$\overline{CS}$ high to SDOUT HI-Z	t_{27}			10	ns
BUSY high in Master Serial Read after Convert[2]	t_{28}		TBD		ns
$\overline{CNVST}$ low to SYNC Asserted Delay (Warp Mode/Normal Mode)	t_{29}		TBD/TBD		ns
SYNC Deasserted to BUSY low Delay	t_{30}		13		ns
Refer to Figure 42 and Figure 43 (Slave Serial Interface Modes)					
External SCLK Setup Time	t_{31}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{32}	2		7	ns
SDIN Setup Time	t_{33}	5			ns
SDIN Hold Time	t_{34}	5			ns
External SCLK Period	t_{35}	12.5[3]			ns
External SCLK high	t_{36}	5			ns
External SCLK low	t_{37}	5			ns

[1] In Warp mode only, the maximum time between conversions is 1ms; otherwise, there is no required maximum time.
[2] In Serial Master Read During Convert mode. See Table 4 for Serial Master Read After Convert Mode. In this mode, the maximum load capacitance on SCLK, SDOUT and SYNC is 10pF.

Table 4. Serial Clock Timings in Master Read After Convert Mode

DIVSCLK[1]		**0**	**0**	**1**	**1**	
DIVSCLK[0]	**Symbol**	**0**	**1**	**0**	**1**	**Unit**
SYNC to SCLK First Edge Delay Minimum	t_{18}	TBD	TBD	TBD	TBD	ns
Internal SCLK Period Minimum	t_{19}	TBD	TBD	TBD	TBD	ns
Internal SCLK Period Maximum	t_{19}	TBD	TBD	TBD	TBD	ns
Internal SCLK High Minimum	t_{20}	TBD	TBD	TBD	TBD	ns
Internal SCLK Low Minimum	t_{21}	TBD	TBD	TBD	TBD	ns
SDOUT Valid Setup Time Minimum	t_{22}	TBD	TBD	TBD	TBD	ns
SDOUT Valid Hold Time Minimum	t_{23}	TBD	TBD	TBD	TBD	ns
SCLK Last Edge to SYNC Delay Minimum	t_{24}	TBD	TBD	TBD	TBD	ns
BUSY High Width Maximum	t_{24}	TBD	TBD	TBD	TBD	µs

ABSOLUTE MAXIMUM RATINGS

Table 5. AD7641 Stress Ratings

Parameter	Rating
Analog Inputs/Outputs	
IN+[4], IN-, REF, REFBUFIN, TEMP, INGND, REFGND to AGND	AVDD + 0.3 V to AGND – 0.3 V
Ground Voltage Differences	
AGND, DGND, OGND	±0.3 V
Supply Voltages	
AVDD, DVDD	–0.3 V to +2.7 V
OVDD	–0.3 V to +3.8 V
Digital Inputs	–0.3 V to 5.5 V
PDREF, PDBUF[5]	±TBDm
Internal Power Dissipation[6]	700 mW
Internal Power Dissipation[7]	2.5 W
Junction Temperature	150°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 10 sec)	300°C

[4] See Analog Inputs section.
[5] See Voltage Reference Input section.
[6] Specification is for the device in free air: 48-Lead LQFP; θ_{JA} = 91°C/W, θ_{JC} = 30°C/W.
[7] Specification is for the device in free air: 48-Lead LFCSP; θ_{JA} = 26°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

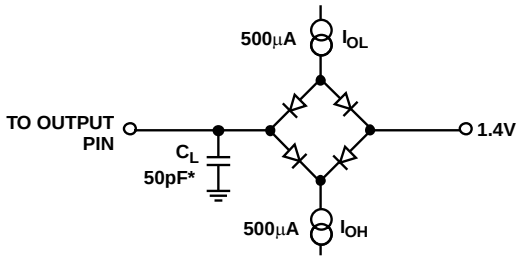


Figure 2. Load Circuit for Digital Interface Timing SDOUT, SYNC, SCLK Outputs, C_L=10 pF

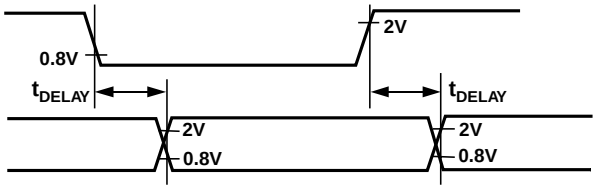


Figure 3. Voltage Reference Levels for Timing

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

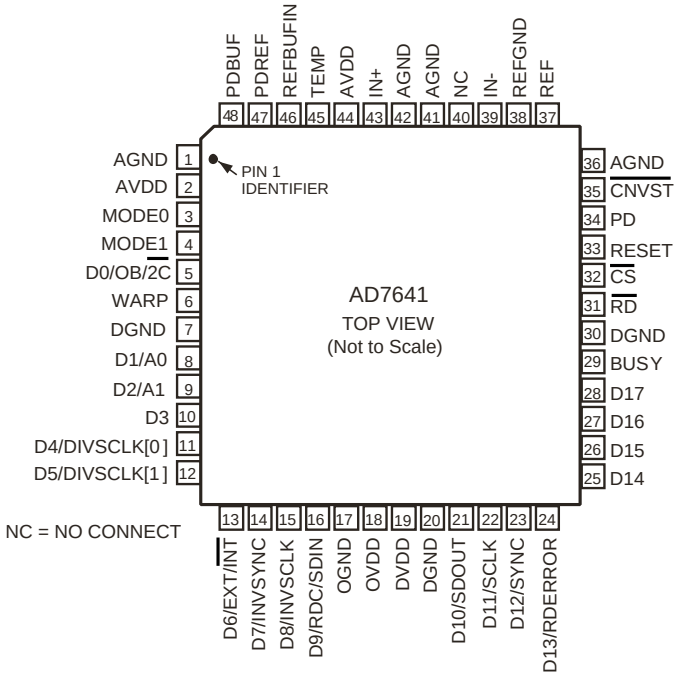


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 36, 41, 42	AGND	P	Analog power ground pin.
2, 44	AVDD	P	Input analog power pins. Nominally 2.5 V
7, 40	NC		No Connect
3, 4	MODE[0:1]	DI	Data Output Interface mode Selection:

Interface MODE #	MODE0	MODE1	Description
0	0	0	18-bit Interface
1	0	1	16-bit Interface
2	1	0	8-bit (Byte) Interface
3	1	1	Serial Interface

5	D0/OB/$\overline{2C}$	DI/O	When MODE=0 (18-bit interface mode), this pin is Bit 0 of the parallel port data output bus and the data coding is straight binary. In all other modes, this pin allows choice of Straight Binary/Binary Two's Complement. When OB/$\overline{2C}$ is HIGH, the digital output is straight binary; when LOW, the MSB is inverted resulting in a two's complement output from its internal shift register.
6	WARP	DI	Conversion mode selection. When HIGH, this input selects the fastest mode, the maximum throughput is achievable, and a minimum conversion rate must be applied in order to guarantee full specified accuracy. When LOW, full accuracy is maintained independent of the minimum conversion rate.
7	DGND	P	Must be tied to Digital Ground
8	D1/A0	DI/O	When MODE=0, this pin is Bit 1 of the parallel port data output bus. In all other modes, this input pin controls the form in which data is output as shown in Table 7.
9	D2/A1	DI/O	When MODE=0, this pin is Bit 2 of the parallel port data output bus. When MODE=1 or MODE=2, this input pin controls the form in which data is output as shown in Table 7.
10	D3	DO	In all modes except MODE=3, this output is used as Bit 3 of the Parallel Port Data Output Bus. This pin is always an output regardless of the interface mode.

Pin No.	Mnemonic	Type[1]	Description
11, 12	D[4:5] or DIVSCLK[0:1]	DI/O	In all modes except MODE=3, these pins are Bit 4 and Bit 5 of the Parallel Port Data Output Bus. In MODE=3 (serial mode), when EXT/$\overline{INT}$ is LOW, and RDC/SDIN is LOW, which serial master read after convert, these inputs, part of the serial port, are used to slow down if desired the internal serial clock clocks the data output. In other serial modes, these pins are not used.
13	D6 or EXT/$\overline{INT}$	DI/O	In all modes except MODE=3, this output is used as Bit 6 of the Parallel Port Data Ouput Bus. When MODE=3 (serial mode), this input, part of the serial port, is used as a digital select input for choosing the internal or an external data clock. With EXT/$\overline{INT}$ tied LOW, the internal clock is selected on SCLK output. With EXT/$\overline{INT}$ set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	D7or INVSYNC	DI/O	In all modes except MODE=3, this output is used as Bit 7 of the Parallel Port Data Output Bus. When MODE=3 (serial mode), this input, part of the serial port, is used to select the active state of the SYNC signal. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.
15	D8 or INVSCLK	DI/O	In all modes except MODE=3, this output is used as Bit 8 of the Parallel Port Data Output Bus. When MODE=3 (serial mode), this input, part of the serial port, is used to invert the SCLK signal. It is active in both master and slave mode.
16	D9 or RDC/SDIN	DI/O	In all modes except MODE=3, this output is used as Bit 9 of the Parallel Port Data Output Bus. When MODE=3 (serial mode), this input, part of the serial port, is used as either an external data input or a read mode selection input depending on the state of EXT/$\overline{INT}$. When EXT/$\overline{INT}$ is HIGH, RDC/SDIN could be used as a data input to daisy chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 18 SCLK periods after the initiation of the read sequence. When EXT/$\overline{INT}$ is LOW, RDC/SDIN is used to select the read mode. When RDC/SDIN is HIGH, the data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data can be output SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply than the supply of the host interface (2.5 V or 3 V).
19	DVDD	P	Digital Power. Nominally at 2.5 V.
20	DGND	P	Digital Power Ground.
21	D10 or SDOUT	DO	In all modes except MODE=3, this output is used as Bit 10 of the Parallel Port Data Output Bus. When MODE=3 (serial mode), this output, part of the serial port, is used as a serial data output synchronized to SCLK. Conversion results are stored in an on-chip shift register. The AD7641 provides the conversion result, MSB first, from its internal shift register. The data format is determined by the logical level of OB/$\overline{2C}$. In serial mode, when EXT/$\overline{INT}$ is LOW, SDOUT is valid on both edges of SCLK. In serial mode, when EXT/$\overline{INT}$ is HIGH: If INVSCLK is LOW, SDOUT is updated SCLK rising edge and valid on the next falling edge. If INVSCLK is HIGH, SDOUT is updated on SCLK falling edge and valid on the next rising edge.
22	D11 or SCLK	DI/O	In all modes except MODE=3, this putput is used as the Bit 11 of the Parallel Port Data Output Bus. When MODE=3 (serial mode), this pin, part of the serial port, is used as a serial data clock input or output, dependent upon the logic state of the EXT/$\overline{INT}$ pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCLK pin.
23	D12 or SYNC	DO	In all modes except MODE=3, this output is used as the Bit 12 of the Parallel Port Data Output Bus. When MODE=3 (serial mode), this output, part of the serial port, is used as a digital output frame synchronization for use with the internal data clock (EXT/$\overline{INT}$ = Logic LOW). When a read sequence is initiated and INVSYNC is LOW, SYNC is driven HIGH and remains HIGH while SDOUT output is valid. When a read sequence is initiated and INVSYNC is HIGH, SYNC is driven LOW and remains LOW while SDOUT output is valid.
24	D13 or RDERROR	DO	In all modes except MODE=3, this output is used as the Bit 12 of the Parallel Port Data Output Bus. In MODE=3 (serial mode) and when EXT/$\overline{INT}$ is HIGH, this output, part of the serial port, is used as a incomplete read error flag. In slave mode, when a data read is started and not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed high.
25-28	D[14:17]	DO	Bit 14 to Bit 17 of the Parallel Port Data output bus. These pins are always outputs regardless of the interface mode.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started, and remains HIGH until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY could be used as a data ready clock signal.

Pin No.	Mnemonic	Type[1]	Description
30	DGND	P	Must be tied to digital ground.
31	$\overline{RD}$	DI	Read Data. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled.
32	$\overline{CS}$	DI	Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{CS}$ is also used to gate the external clock.
33	RESET	DI	Reset Input. When set to a logic HIGH, reset the AD7641. Current conversion if any is absorbed. If not used, this pin could be tied to the DGND.
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current one is completed.
35	$\overline{CNVST}$	DI	Start Conversion. A falling edge on CNVST puts the internal sample/hold into the hold state and initiates a conversion.
37	REF	AI	Reference Input Voltage and Internal Reference Buffer Output. Apply an external reference on this pin if the internal reference buffer is not used. Should be decoupled effectively with or without the internal buffer.
38	REFGND	AI	Reference Input Analog Ground.
39	IN-	AI	Differential Negative Analog Input.
43	IN+	AI	Differential Negative Analog Input.
45	TEMP	AO	Temperature sensor analog output.
46	REFBUFIN	AI	Internal Reference Output and Reference Buffer Input Voltage. The internal reference buffer has a fixed gain. It outputs 2.048V typically when 1.2V is applied on this pin.
47	PDREF	DI	This pin allows the choice of internal or external voltage references. When LOW, the on-chip reference is turned on. When HIGH, the internal reference is switched off and an external reference must be used.
48	PDBUF	DI	This pin allows the choice of buffering an internal or external reference with the internal buffer. When LOW, the buffer is selected. When HIGH, the buffer is switched off.

[1] AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital Input; DI/O = bidirectional digital; DO = digital output; P = Power.

Table 7. Data Bus Interface Definition

MODE	MODE1	MODE0	D0/OB/$\overline{2C}$	D1/A0	D2/A1	D[3]	D[4:9]	D[10:11]	D[12:15]	D[16:17]	DESCRIPTION
0	0	0	R[0]	R[1]	R[2]	R[3]	R[4:9]	R[10:11]	R[12:15]	R[16:17]	18-Bit Parallel
1	0	1	OB/$\overline{2C}$	A0:0	R[2]	R[3]	R[4:9]	R[10:11]	R[12:15]	R[16:17]	16-Bit High Word
1	0	1	OB/$\overline{2C}$	A0:1	R[0]	R[1]	All Zeros				16-Bit Low Word
2	1	0	OB/$\overline{2C}$	A0:0	A1:0	All Hi-Z		R[10:11]	R[12:15]	R[16:17]	8-Bit HIGH Byte
2	1	0	OB/$\overline{2C}$	A0:0	A1:1	All Hi-Z		R[2:3]	R[4:7]	R[8:9]	8-Bit MID Byte
2	1	0	OB/$\overline{2C}$	A0:1	A1:0	All Hi-Z		R[0:1]	All Zeros		8-Bit LOW Byte
2	1	0	OB/$\overline{2C}$	A0:1	A1:1	All Hi-Z		All Zeros		R[0:1]	8-Bit LOW Byte
3	1	1	OB/$\overline{2C}$	All Hi-Z		Serial Interface					Serial Interface

R[0:17] is the 18-bit ADC value stored in its output register.

TERMINOLOGY

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Gain Error
The first transition (from 000…00 to 000…01) should occur for an analog voltage 1/2 LSB above the nominal negative full scale (−2.0479922 V for the ±2.048V range). The last transition (from 111…10 to 111…11) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (2.0479766 V for the ±2.048V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Zero Error
The zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Signal to (Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious Free Dynamic Range (SFDR)
The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and is expressed in bits by the following formula:

$$ENOB = (SINAD_{dB} - 1.76)/6.02)$$

Aperture Delay
Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the $\overline{\text{CNVST}}$ input to when the input signal is held for a conversion.

Transient Response
The time required for the AD7621 to achieve its rated accuracy after a full-scale step function is applied to its input.

Reference Voltage Temperature Coefficient
Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts maximum and minimum reference output voltage (VREF) measured at TMIN, T(25°C), and TMAX. It is expressed in ppm/°C using the following equation:

$$TCV_{REF}(\text{ppm/°C}) = \frac{V_{REF}(Max) - V_{REF}(Min)}{V_{REF}(25°C) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
$V_{REF}(Max)$ = Maximum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}
$V_{REF}(Min)$ = Minimum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}
$V_{REF}(25°C)$ = V_{REF} at 25°C
T_{MAX} = +85°C
T_{MIN} = −40°C

Thermal Hysteresis
Thermal hysteresis is defined as the absolute maximum change of reference output voltage after the device is cycled through temperature from either

T_HYS+ = 25°C to T_{MAX} to 25°C
T_HYS- = 25°C to T_{MIN} to 25°C

It is expressed in ppm using the following equation:

$$V_{HYS}(ppm) = \left| \frac{V_{REF}(25°C) - V_{REF}(T\_HYS)}{V_{REF}(25°C)} \right| \times 10^6$$

where:
$V_{REF}(25°C)$ = V_{REF} at 25°C
$V_{REF}(T\_HYS)$ = Maximum change of V_{REF} at T_HYS+ or T_HYS−

TYPICAL PERFORMANCE CHARACTERISTICS

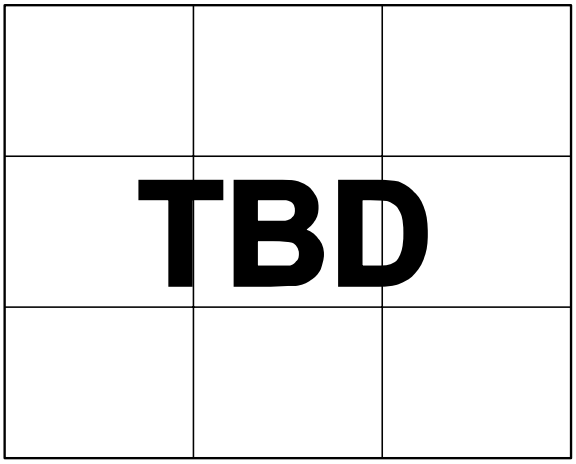


Figure 5. Integral Nonlinearity vs. Code

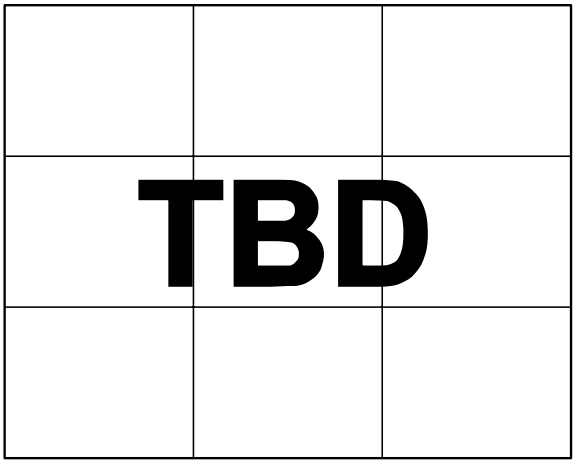


Figure 8. Differential Nonlinearity vs. Code

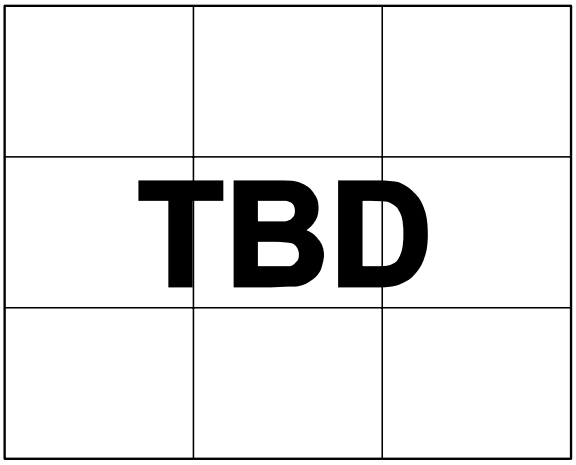


Figure 6.Typical Positive INL Distribution (TBD Units)

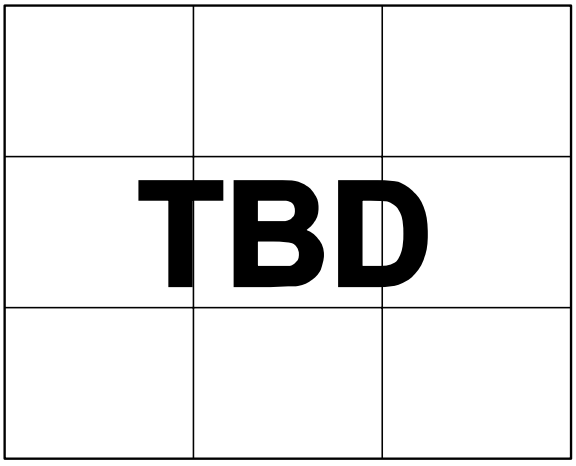


Figure 9. .Typical negative INL Distribution (TBD Units)

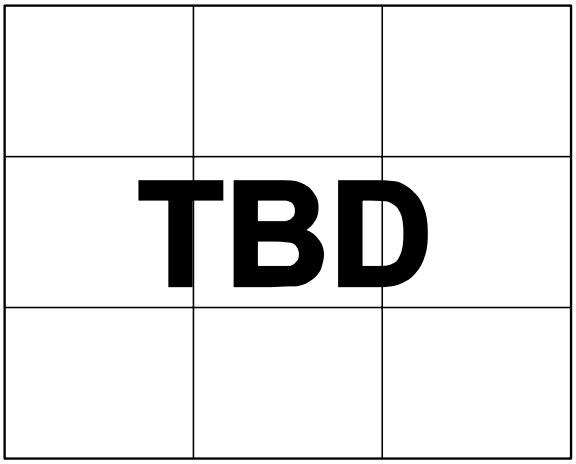


Figure 7. Typical Positive DNL Distribution (TBD Units)

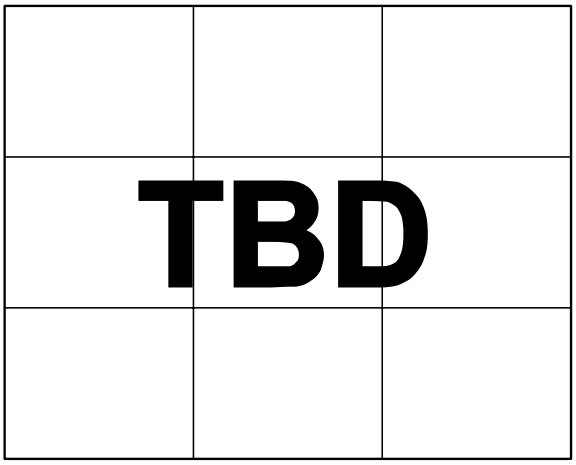


Figure 10. Typical Negative DNL Distribution (TBD Units)

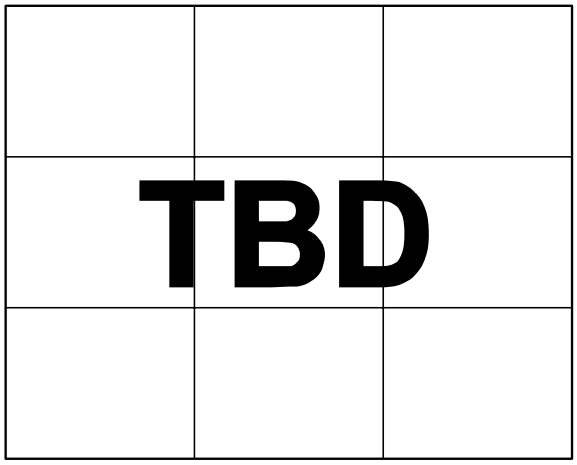


Figure 11. Histogram of 261,120 Conversions of a DC Input at the Code Transition

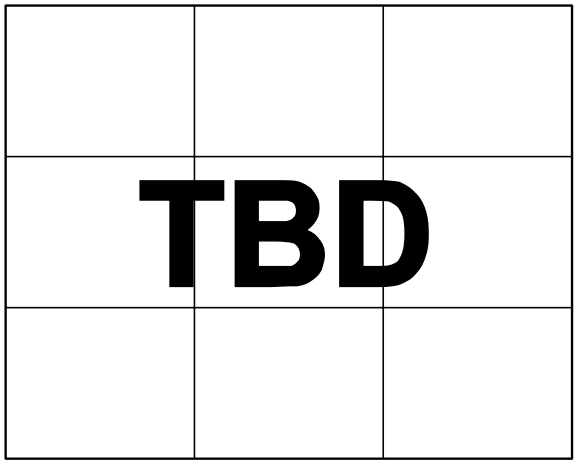


Figure 12. FFT Plot

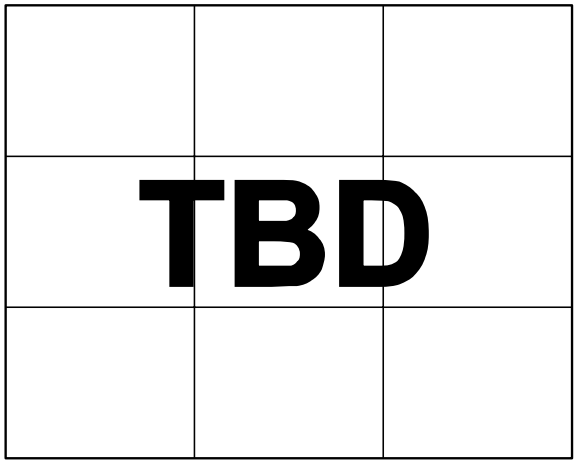


Figure 13. SNR, S/(N+D) and ENOB vs. Frequency

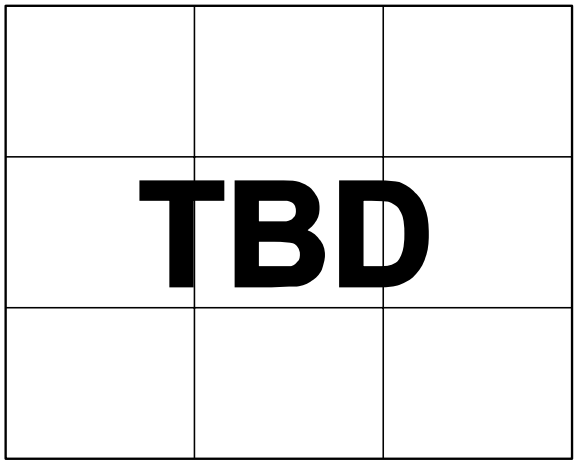


Figure 14. Histogram of 261,120 Conversions of a DC Input at the Code Center

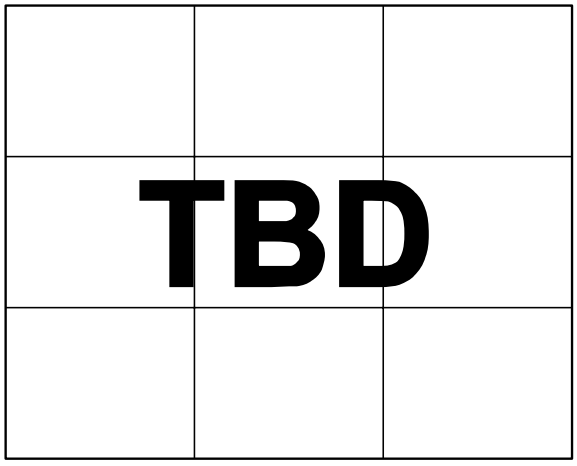


Figure 15. THD, Harmonics, and SFDR vs. Frequency

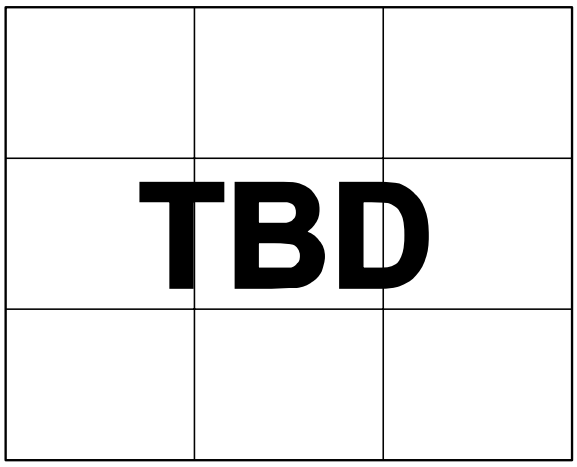


Figure 16. SNR, S/(N+D) and THD vs. Input Level (Referred to Full Scale)

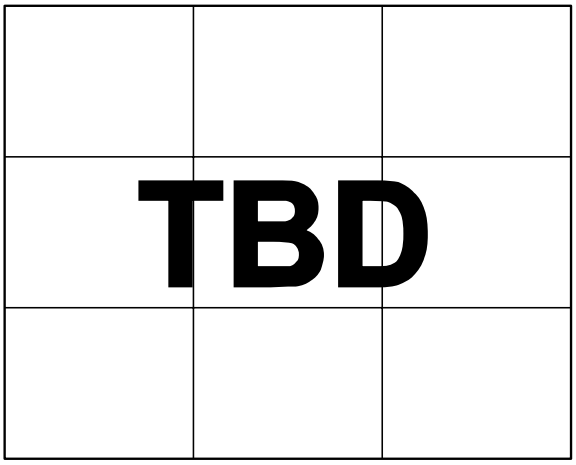


Figure 17. SNR, S/(N+D), SFDR, and ENOB vs. Temperature

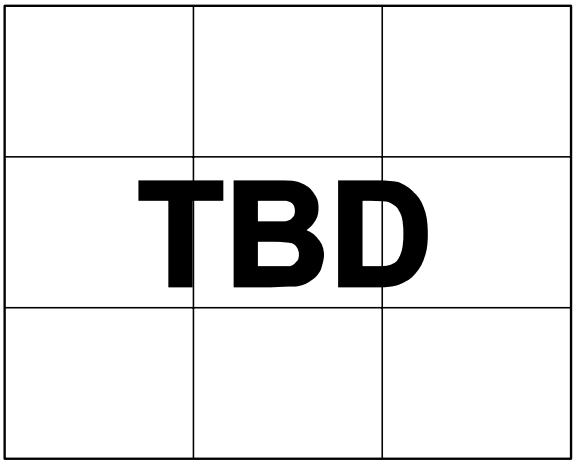


Figure 20. Zero Error, Gain Error with Reference vs. Temperature

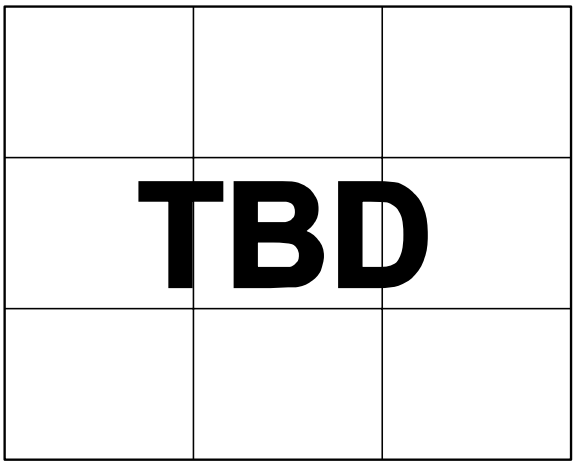


Figure 18. THD and Harmonics vs Temperature

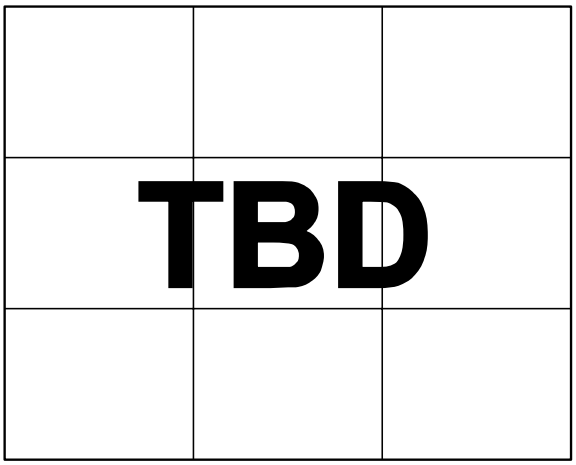


Figure 21. Typical Reference Voltage Output vs. Temperautre

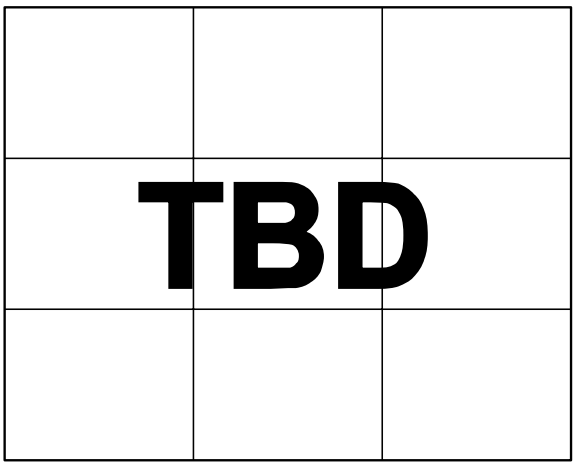


Figure 19. Operating Current vs. Sample Rate

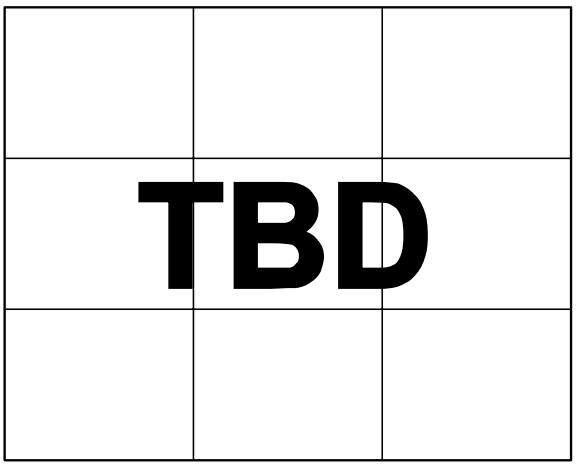
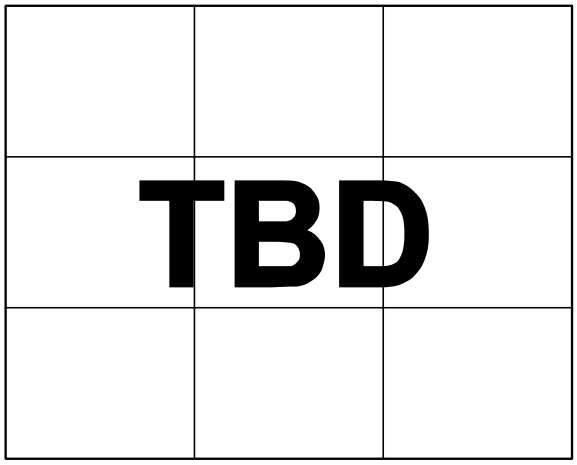


Figure 22. Reference Voltage Temperature Coefficient Distribution (TBD Units)



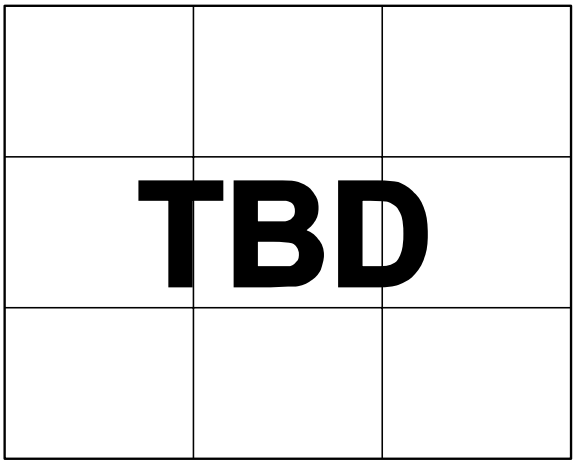


Figure 23. Typical Delay vs. Load Capacitance CL

APPPLICATIONS INFORMATION

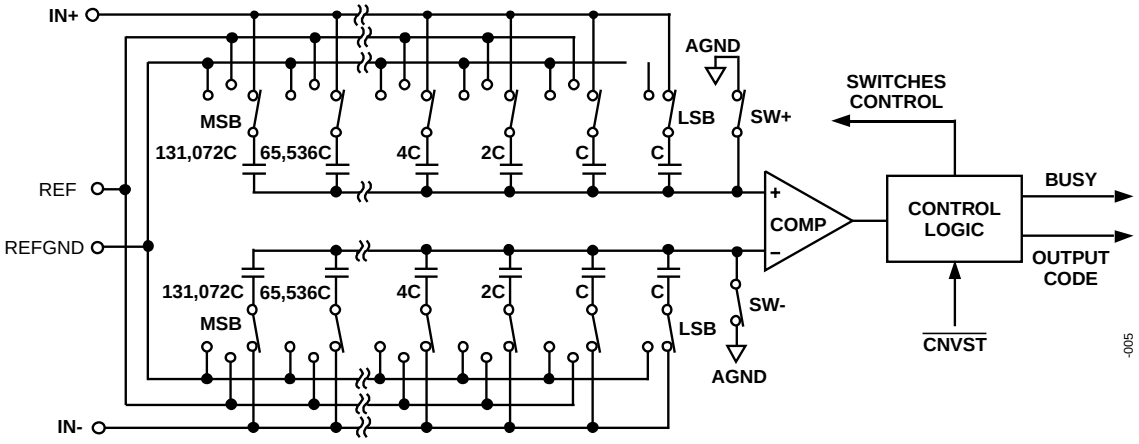


Figure 24. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7641 is a very fast, low-power, single-supply, precise 18-bit analog-to-digital converter (ADC) using successive approximation architecture. The AD7641 features different modes to optimize performances according to the applications. In Warp mode, the AD7641 is capable of converting 2,000,000 samples per second (2 MSPS).

The AD7641 provides the user with an on-chip track/hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7641 can be operated from a single 2.5 V supply and be interfaced to either 5 V or 3.3 V or 2.5 V digital logic. It is housed in a 48-lead LQFP or a tiny LFCSP packages that combines space savings and allows flexible configurations as either serial or parallel interface. The AD7641 is pin-to-pin-compatible and is a speed upgrade of the AD7674.

CONVERTER OPERATION

The AD7641 is a successive approximation analog-to-digital converter based on a charge redistribution DAC. Figure 24 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 18 binary weighted capacitors which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to AGND via SW+ and SW-. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on IN+ and IN- inputs. When the acquisition phase is complete and the $\overline{\text{CNVST}}$ input goes low, a conversion phase is initiated. When the conversion phase begins, SW+ and SW- are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between the inputs IN+ and IN- captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFGND or REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ . . . $V_{REF}/262144$). The control logic toggles these switches, starting with the MSB first, in order to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and brings BUSY output low.

MODES OF OPERATION

The AD7641 features two modes of operations; Warp and Normal. Each of these modes is more suitable for specific applications.

The Warp mode (Warp = high) allows the fastest conversion rate up to 2 MSPS. However, in this mode, and this mode only, the full specified accuracy is guaranteed only when the time between conversions does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms (e.g. after power-up) the first conversion result should be ignored. This mode makes the AD7641 ideal for applications where both high accuracy and fast sample rate are required.

The Normal mode is the fastest mode (1.5 MSPS) without any limitation about the time between conversions. This mode makes the AD7641 ideal for asynchronous applications such as data acquisition systems, where both high accuracy and fast sample rate are required.

TRANSFER FUNCTIONS

Except in 18 Bit interface mode, using the OB/$\overline{2C}$ digital input, the AD7641 offers two output codings: straight binary and two's complement. The LSB size with V_{REF} = 2.048V is 2*V_{REF}/262,144 which is 15.63uV. Refer to Figure 25and Table 8 for the ideal transfer characteristic.

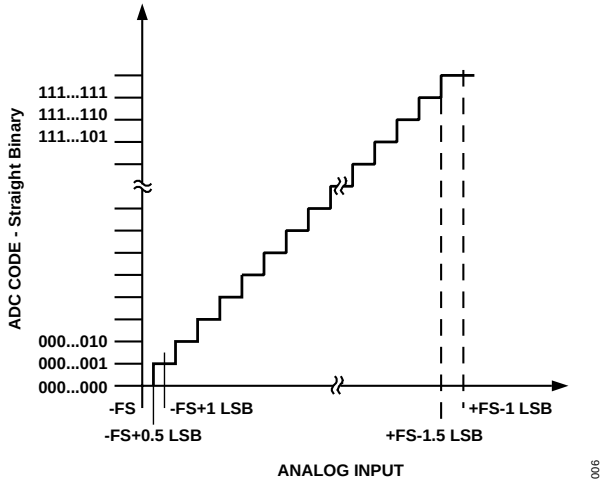


Figure 25. ADC Ideal Transfer Function

Table 8. Output Codes and Ideal Input Voltages

Description	Digital Output Code (Hex)		
	Analog Input V_{REF}= 2.048V	Straight Binary	Twos Complement
FSR –1 LSB	2.047984 V	3FFFF[8]	1FFFF[1]
FSR – 2 LSB	2.047969 V	3FFFE	1FFE
Midscale + 1 LSB	15.625µV	20001	00001
Midscale	0 V	20000	00000
Midscale – 1 LSB	-15.625µV	1FFFF	3FFFF
-FSR + 1 LSB	-2.047984 V	00001	20001
-FSR	-2.048 V	00000[9]	20000[2]

[8] This is also the code for overrange analog input (V_{IN+} – V_{IN-} above V_{REF} – V_{REFGND}).

[9] This is also the code for underrange analog input (V_{IN+} – VI_{N-} below -V_{REF} + V_{REFGND}).

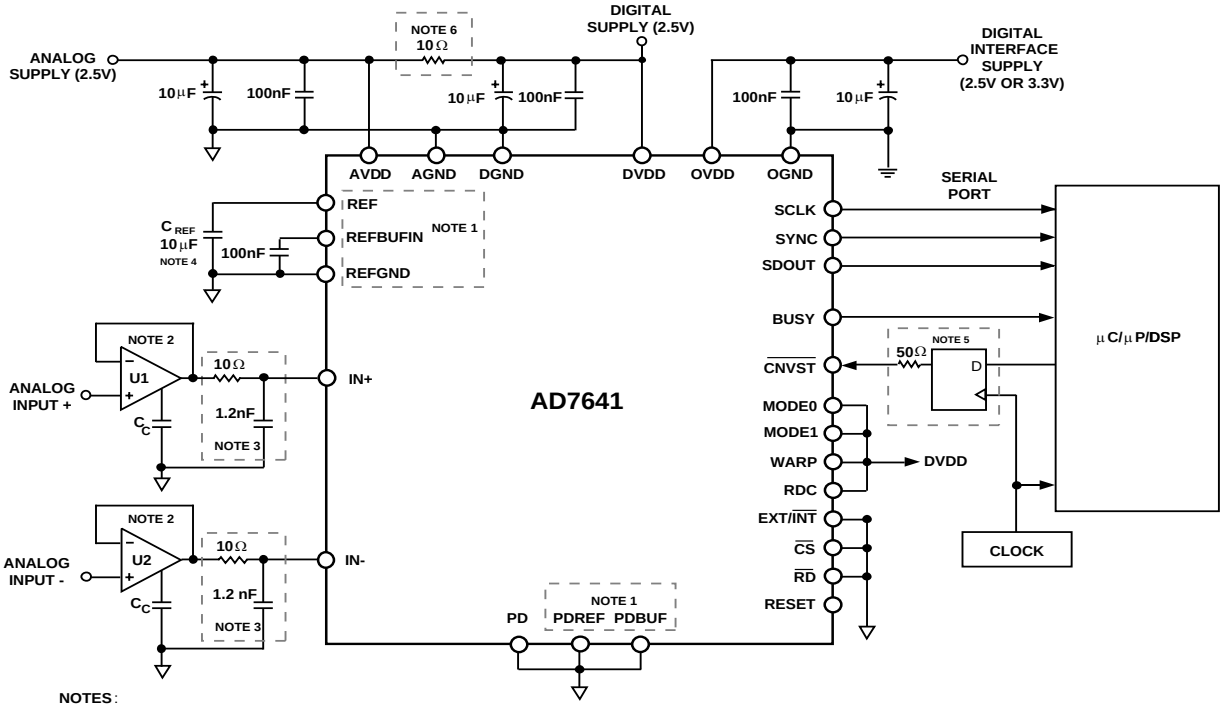


Figure 26. Typical Connection Diagram (Internal reference buffer, serial interface)

TYPICAL CONNECTION DIAGRAM

Figure 26 shows a typical connection diagram for the AD7641. Different circuitry shown on this diagram are optional and are discussed below.

ANALOG INPUTS

Figure 27 shows a simplified analog input section of the AD7641.

The two diodes, D1 and D2, provide ESD protection for the analog inputs IN+and IN-. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V. This will cause these diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of TBD mA maximum. For instance, these conditions could eventually occur when the input buffer's U1 or U2 supplies are different from AVDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the device.

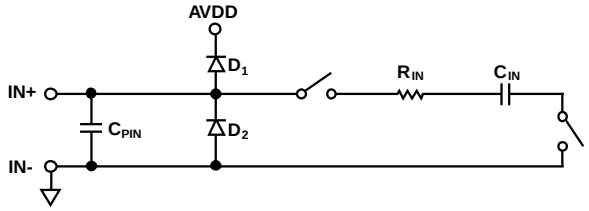


Figure 27. AD7641 simplified Analog input

This analog input is a true differential structure. By using this differential input, small signals common to both inputs are rejected, as shown in Figure 28, which represents the typical CMRR over frequency with on-chip and external references.

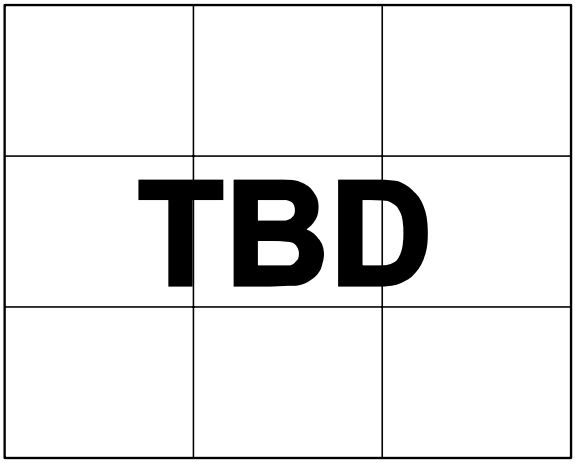


Figure 28. Analog Input CMRR vs. Frequency

During the acquisition phase for AC singals, the impedance of the analog inputs IN+ and IN- can be modeled as a parallel combination of capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically TBD Ω and is a lumped component made up of some serial resistors and the on resistance of the switches. C_{IN} is typically 12 pF and is mainly the ADC sampling capacitor. During the conversion phase, where the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole low-pass filter has a typical −3dB cutoff frequency of 50 MHz which reduces undesirable aliasing effect and limits the noise coming from the inputs.

Since the input impedance of the AD7641 is very high, the AD7641 can be driven directly by a low impedance source without gain error. To further improve the noise filtering done by the AD7641 analog input circuit, an external one-pole RC filter between the amplifiers outputs and the ADC analog inputs can be used as shown in Figure 26 However, large source impedances significantly affect the ac performance, especially total harmonic distortion (THD). The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency, as shown in Figure 29.

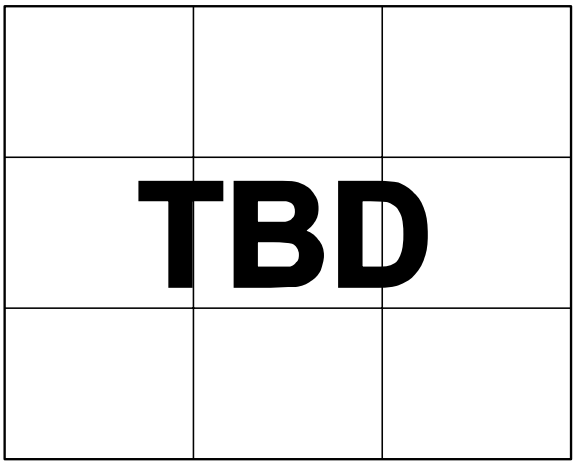


Figure 29. THD vs. Analog Input Frequency and Source Resistance

DRIVER AMPLIFIER CHOICE

Although the AD7641 is easy to drive, the driver amplifier needs to meet at least the following requirements:

- The driver amplifier and the AD7641 analog input circuit together, must be able to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%). In the amplifier's data sheet, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection. The AD8021 op amp, which combines ultra low noise (2.1nV/√Hz) and high gain-bandwidth, meets this settling time requirement even when used with gains up to 13.

- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7641. The noise coming from the driver is filtered by the AD7641 analog input circuit 1-pole low-pass filter made by R_{IN} and C_{IN} or by the external filter, if one is used. The SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20LOG\left(\frac{38}{\sqrt{1444 + \pi f_{-3dB}\left(Ne_N\right)^2}}\right)$$

where:

f_{-3dB} is the input bandwidth of the AD7641 (50 MHz) or the cutoff frequency of the RC input filter (13.3 MHz), if one is used.

N is the noise factor of the amplifier (+1 in buffer configuration).

e_N is the equivalent input voltage noise density of the op amp, in nV/√Hz.

For instance, a driver with an equivalent input noise density of 2.1 nV/√Hz, like the AD8021, with a noise gain of +1 when configured as a buffer, degrades the SNR by only 0.52 dB when using the RC filter in Figure 26 and by 1.7 dB without the filter.

- The driver needs to have a THD performance suitable to that of the AD7641. Figure 15 gives the THD versus frequency that the driver should exceed.

The AD8021 meets these requirements and is appropriate for almost all applications. The AD8021 needs a 10 pF external compensation capacitor that should have good linearity as an NPO ceramic or mica type. Moreover, the use of a noninverting +1 gain arrangement is recommended and helps to obtain the best signal-to-noise ratio.

The AD8022 could also be used if a dual version is needed and gain of 1 is present. The AD829 is an alternative in applications where high frequency (above 100 kHz) performance is not required. In gain of 1 applications, it requires an 82 pF compensation capacitor. The AD8610 is an option when low bias current is needed in low frequency applications.

Single to Differential Driver

For applications using unipolar analog signals, a single-ended to differential driver will allow for a differential input into the part. The schematic is shown in Figure 30. This configuration, when provided an input signal of 0 to V_{REF} , will produce a differential ± V_{REF} with mid-scale at $V_{REF}/2$. The 1-pole filter using R= 10 Ω and C= 1.2nF provides a corner frequency of 13.3MHz.

If the application can tolerate more noise, the AD8139, differential driver, can be used.

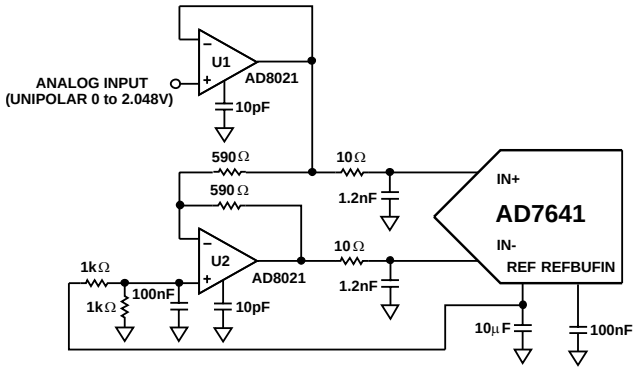


Figure 30. Single Ended to Differential Driver Circuit (Internal Reference Used)

VOLTAGE REFERENCE INPUT

The AD7641 allows the choice of either a very low temperature drift internal voltage reference or an external reference.

Unlike many ADCs with internal references, the internal reference of the AD7641 provides excellent performance and can be used in almost all applications.

Internal Reference (PDBUF = Low , PDREF = Low)

To use the internal reference, the PDREF and PDBUF inputs should both be low. This produces the 1.2 V bandgap output on REFBUFIN which, amplified by the buffer, results in a 2.048 V reference on the REF pin.

The output resistance of the REFBUFIN is 6.33 kΩ (minimum) when the internal reference is enabled. It is necessary to decouple this with a ceramic capacitor greater than 100 nF. Thus the capacitor provides an RC filter for noise reduction.

External Reference and Internal Buffer (PBBUF =Low, PDREF = High)

To use an external reference along with the internal buffer, PDREF should be high and PDBUF should be low. This powers down the internal reference and allows the 1.2V reference to be applied to REFBUFIN.

External Reference (PDBUF =High, PRBUF = High)

To use an external reference directly on REF pin, PDREF and PDBUF should both be high.

PDREF and PDBUF power down the internal reference and the internal reference buffer, respectively. Note that the PDREF and PDBUF input current should never exceed 20 mA. This could eventually occur when input voltage is above AVDD (for instance, at power-up). In this case, a 100 Ω series resistor is recommended.

The internal reference is temperature compensated to 2.048 V ±TBD mV. The reference is trimmed to provide a typical drift of

3 ppm/°C . This typical drift characteristic is shown in Figure 22. For improved drift performance, an external reference, such as the AD780 or ADR431, can be used.

However, the advantages of using the external voltage reference directly are:

- The SNR and dynamic range improvement (about 1.7 dB) resulting form the use of a reference voltage very close to the supply (2.5V) instead of a typical 2.048 reference when the internal reference is used. This is calculated by:

$$SNR = 20Log\left(\frac{2.048}{2.50}\right)$$

- The power savings when the internal reference is powered down (PBREF high).

In both cases, the AD7641 voltage reference input REF has a dynamic input impedance; it should therefore be driven by a low impedance source with efficient decoupling between the REF and REFGND inputs. This decoupling depends on the choice of the voltage reference but usually consists of a low ESR tantalum capacitor connected to REF and REFGND with minimum parasitic inductance. A 10 µF (X5R, 1206 size) ceramic chip capacitor (or 47 µF tantalum capacitor) is appropriate when using either the internal reference or one of these recommended reference voltages:

- The low noise, low temperature drift ADR431 and AD780
- The low power ADR291
- The low cost AD1582

For applications that use multiple AD7621s, it is more effective to use the internal buffer to buffer the reference voltage.

Care should be taken with the voltage reference's temperature coefficient, (TC) which directly affects the full-scale accuracy if this parameter matters. For instance, a ±4 ppm/°C TC of the reference changes full scale by ±1 LSB/°C.

Note that V_{REF} can be increased to AVDD + 0.1V. Since the input range is defined in terms of V_{REF}, this would essentially increase the range to 0 V to 2.8V with an AVDD = 2.7V.

Temperature Sensor

The TEMP pin, which measures the temperature of the AD7621, can be used as shown in Figure 31. The output of TEMP pin is applied to one of the inputs of the analog switch (e.g., ADG779), and the ADC itself is used to measure its own temperature. This configuration is very useful for improving the calibration accuracy over the temperature range.

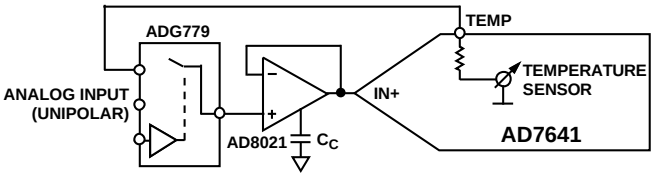


Figure 31. Use of the Temperature Sensor

POWER SUPPLY

The AD7641 uses three sets of power supply pins: an analog 2.5V supply AVDD, a digital 2.5 V core supply DVDD, and a digital input/output interface supply OVDD. The OVDD supply allows direct interface with any logic working between 2.3 V and 5.25 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply as shown in Figure 26. The AD7641 is independent of power supply sequencing and thus free from supply voltage induced latchup. Additionally, it is very insensitive to power supply variations over a wide frequency range as shown in Figure 32.

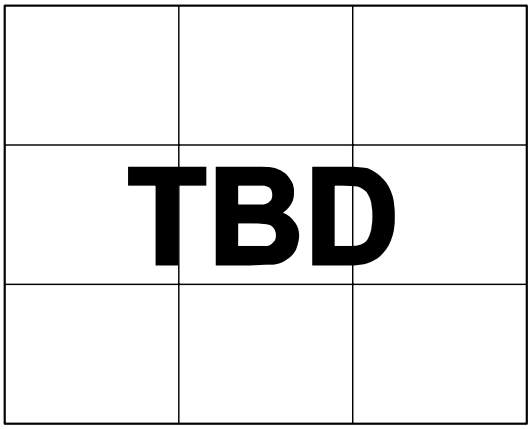


Figure 32. PSRR vs. Frequency

CONVERSION CONTROL

Figure 33 shows the detailed timing diagrams of the conversion process. The AD7641 is controlled by the signal $\overline{CNVST}$ which initiates conversion. Once initiated, it cannot be restarted or aborted, even by the power-down input, PD, until the conversion is complete. The $\overline{CNVST}$ signal operates independently of $\overline{CS}$ and $\overline{RD}$ signals.

In most cases, the $\overline{CNVST}$ signal cannot be a 50% duty cycle clock since the rising edge can occur during critical bit decisions. Since the AD7641 has error correction circuitry during the beginning of BUSY = high, it is recommended to keep the $\overline{CNVST}$ rising edge within this time. Since the $\overline{CNVST}$ low to BUSY high delay (t3) has a maximum of 30ns, there is no guarantee to time the rising edge from this time thus the best is to provide a $\overline{CNVST}$ pulse with the low time < 70ns.

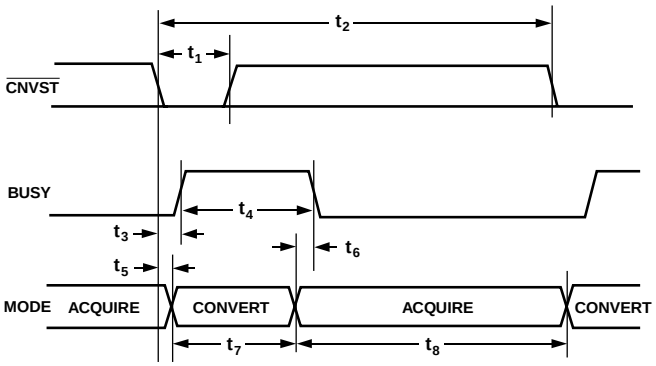


Figure 33. Basic Conversion Timing

Although $\overline{\text{CNVST}}$ is a digital signal, it should be designed with special care with fast, clean edges, and levels with minimum overshoot and undershoot or ringing.

The $\overline{\text{CNVST}}$ trace should be shielded with ground and a low value serial resistor (e.g., 50 Ω) termination should be added close to the output of the component that drives this line.

For applications where SNR is critical, the $\overline{\text{CNVST}}$ signal should have very low jitter. This can be achieved by using a dedicated oscillator for $\overline{\text{CNVST}}$ generation, or by clocking $\overline{\text{CNVST}}$ with a high frequency, low jitter clock, as shown in Figure 26.

DIGITAL INTERFACE

The AD7641 has a versatile digital interface; it can be interfaced with the host system by using either a serial or parallel interface. The serial interface is multiplexed on the parallel data bus. The AD7641 digital interface also accommodates both 2.5V, 3.3V or 5V logic with either OVDD at 2.5V or 3.3V. OVDD defines the logic high output voltage. In most applications, the OVDD supply pin of the AD7641 is connected to the host system interface 2.5V or 3.3V digital supply. Finally, by using the OB/$\overline{\text{2C}}$ input pin, either two's complement or straight binary coding can be used. Please refer to Table 7 for a detailed description of the different options available.

The two signals $\overline{\text{CS}}$ and $\overline{\text{RD}}$ control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{\text{CS}}$ allows the selection of each AD7621 in multi-circuits applications and is held low in a single AD7621 design. $\overline{\text{RD}}$ is generally used to enable the conversion result on the data bus.

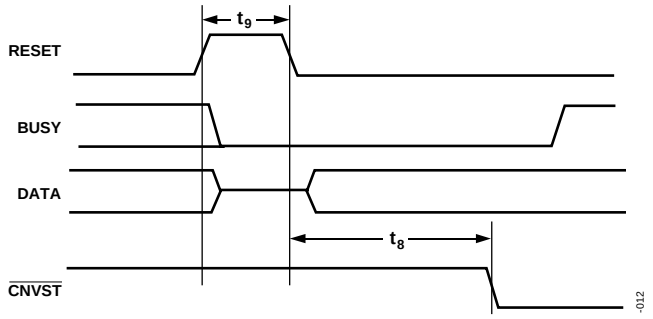


Figure 34. RESET Timing

PARALLEL INTERFACE

The AD7641 is configured to use the parallel interface with either an 18-bit, 16-bit or 8-bit bus width according to the Table 7. The AD7641 is configured to use the parallel interface in either MODE0, MODE1 or MODE2 for 18-bit, 16-bit and 8-bit interfaces respectively.

Master Parallel Interface

Data can be read continuously by tying $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low thus requiring minimal microprocessor connections. However, in this mode the data bus is always driven and cannot be used in shared bus applications (unless the device is held in RESET). Figure 35 details the timing for this mode.

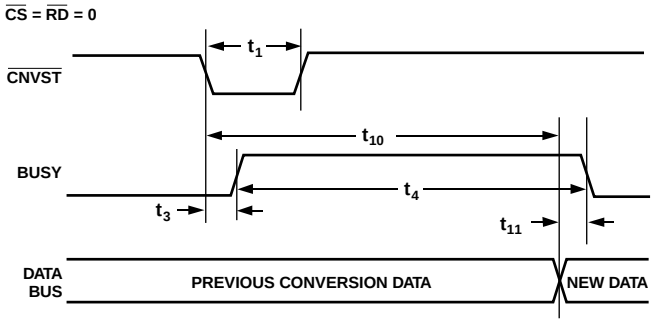


Figure 35. Master Parallel Data Timing for Reading (Continuous Read)

Slave Parallel Interface

In slave parallel reading mode, the data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion, as shown in Figure 36 and Figure 37 respectively. When the data is read during the conversion, however, it is recommended that it is read only during the first half of the conversion phase. This avoids any potential feed through between voltage transients on the digital interface and the most critical analog conversion circuitry.

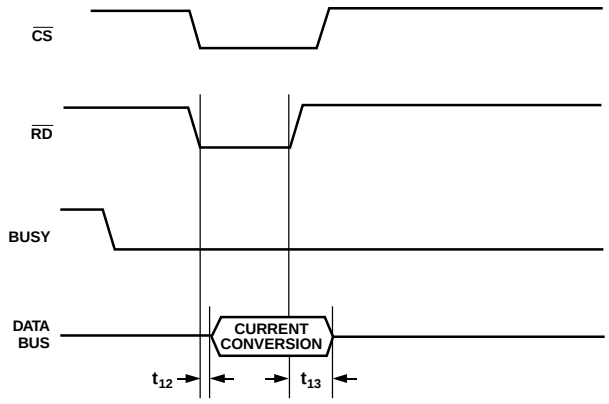


Figure 36. Slave Parallel Data Timing for Reading (Read After Convert)

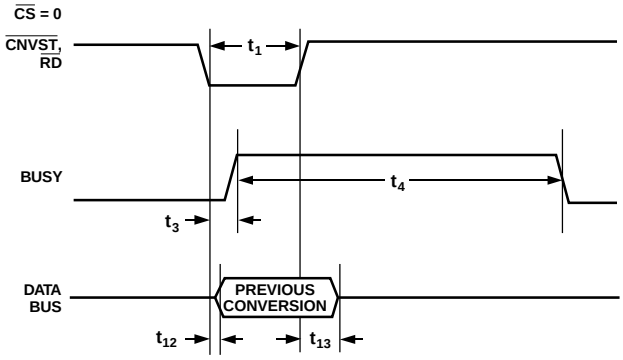


Figure 37. Slave Parallel Data Timing for Reading (Read During Convert)

16-bit and 8-Bit Interface (Master or Slave)

When using the 16-bit and 8-bit interface modes (MODE = 1, MODE = 2 respectively) the A0 and A1 pins control which word or byte of data is available on the bus. Refer to Table 7 for the explicit details of these modes. For the 16-bit interface, two consecutive reads are required to read the 18 bits of data on D[2:17] using A0. For the 8-bit (byte) interface, three consecutive reads are required to read the 18 bits of data on D[10:17]. This interface can be used in both master and slave parallel reading modes. Figure 38 details the timing for these modes.

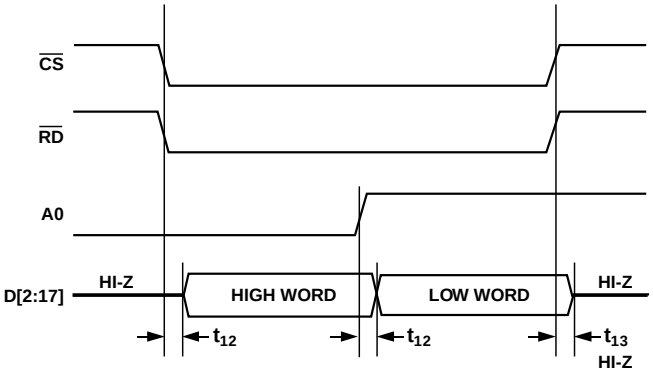


Figure 38. 8-Bit and 16-Bit Parallel Interface (16-bit shown)

SERIAL INTERFACE

The AD7641 is configured to use the serial interface in MODE = 3 (MODE0 = MODE1 = high). The AD7641 outputs 18 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 18 clock pulses provided on SCLK pin. The output data is valid on both the rising and falling edge of the data clock.

MASTER SERIAL INTERFACE

Internal Clock

The AD7641 is configured to generate and provide the serial data clock SCLK when the D6/EXT/$\overline{\text{INT}}$ pin is held low. The AD7641 also generates a SYNC signal to indicate to the host when the serial data is valid. The SCLK and SYNC signals can be inverted, if desired, by driving the INVSCLK and INVSYNC pins high. Depending on the read during convert input, RDC/SDIN, the data can be read after each conversion or during the following conversion. Figure 39 and Figure 40 show detailed timing diagrams of these two modes. To accommodate slow digital hosts, the serial clock can be slowed down by using DIVSCLK[0:1] pins. Refer to Table 4 for timing details.

Usually, because the AD7641 is used with a fast throughput, the Master Read During Conversion mode is the most recommended serial mode. In this mode, the serial clock and data toggle at appropriate instants, minimizing potential feed through between digital activity and critical conversion decisions. Note that in this mode, the SCLK period changes since the LSBs require more time to settle and the SCLK is derived from the SAR conversion cycle.

In Read After Conversion mode, it should be noted that unlike in other modes, the BUSY signal returns low after the 18 data bits are pulsed out and not at the end of the conversion phase, which results in a longer BUSY width.

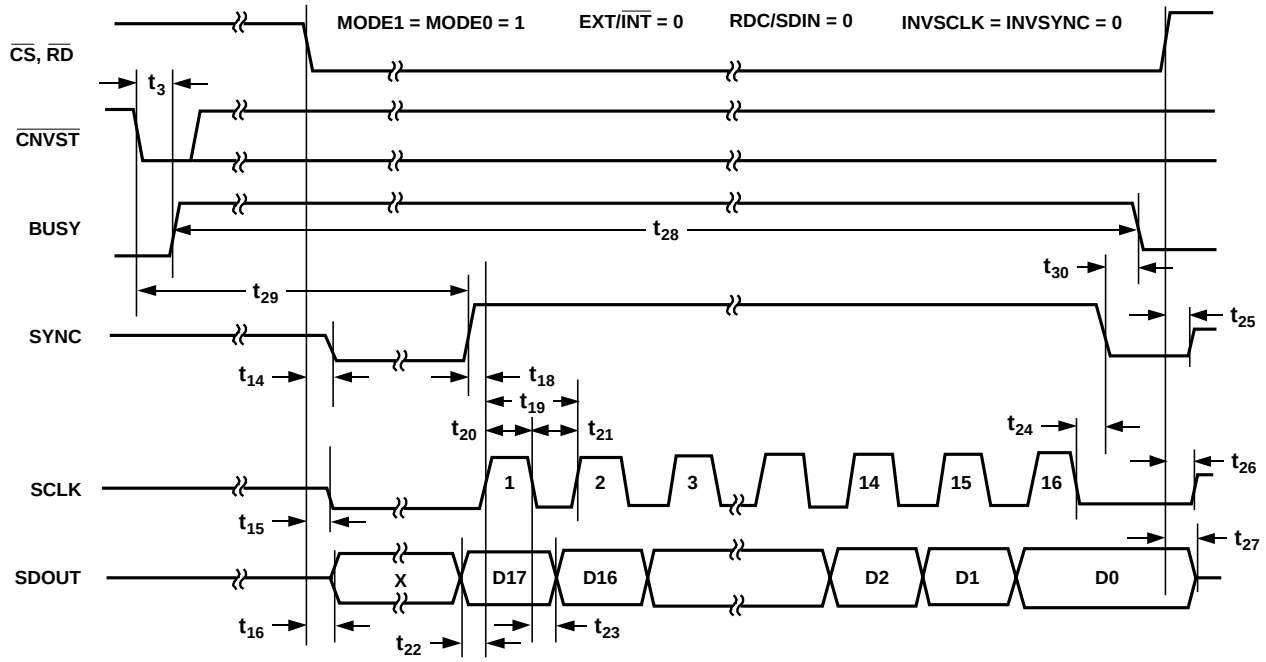


Figure 39. Master Serial Data Timing for Reading (Read After Convert)

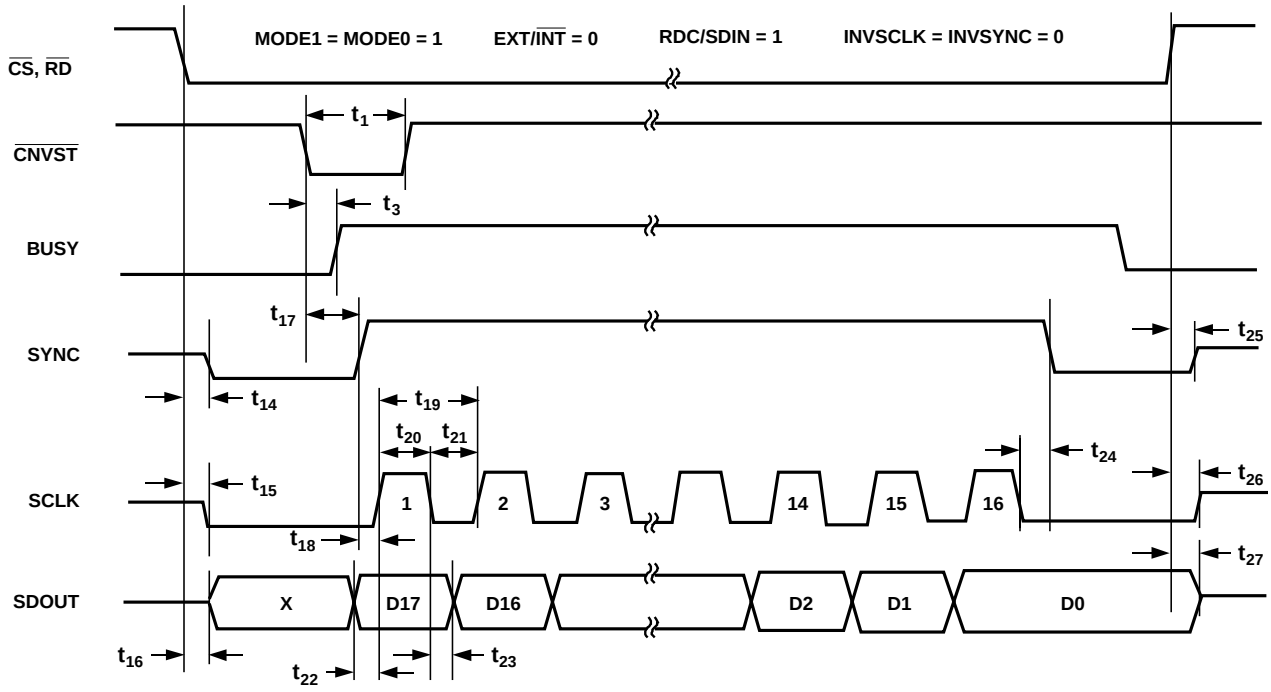


Figure 40. Master Serial Data Timing for Reading (Read Previous Conversion During Convert)

SLAVE SERIAL INTERFACE

External Clock

The AD7641 is configured to accept an externally supplied serial data clock on the SCLK pin when the D6/EXT/$\overline{INT}$ pin is held high. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{CS}$. When $\overline{CS}$ and $\overline{RD}$ are both low, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or a discontinuous clock. A discontinuous clock can be either normally high or normally low when inactive. Figure 42 and Figure 43 show the detailed timing diagrams of these methods.

While the AD7641 is performing a bit decision, it is important that voltage transients be avoided on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because the AD7641 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that is toggling only when BUSY is low or, more importantly, that it does not transition during the latter half of BUSY high.

External Discontinuous Clock Data Read After Conversion

Though the maximum throughput cannot be achieved using this mode, it is the most recommended of the serial slave modes. Figure 42 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by BUSY returning low, the conversion result can be read while both $\overline{CS}$ and $\overline{RD}$ are low. Data is shifted out MSB first with 16 clock pulses and is valid on the rising and falling edges of the clock.

Among the advantages of this method is the fact that conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process. Another advantage is the ability to read the data at any speed up to 80 MHz, which accommodates both the slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7641 provides a daisy-chain feature using the RDC/SDIN pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when desired, as, for instance, in isolated multi-converter applications.

An example of the concatenation of two devices is shown in Figure 41. Simultaneous sampling is possible by using a common $\overline{CNVST}$ signal. It should be noted that the RDC/SDIN input is latched on the edge of SCLK opposite to the one used to shift out the data on SDOUT. Hence, the MSB of the "upstream" converter just follows the LSB of the "downstream" converter on the next SCLK cycle.

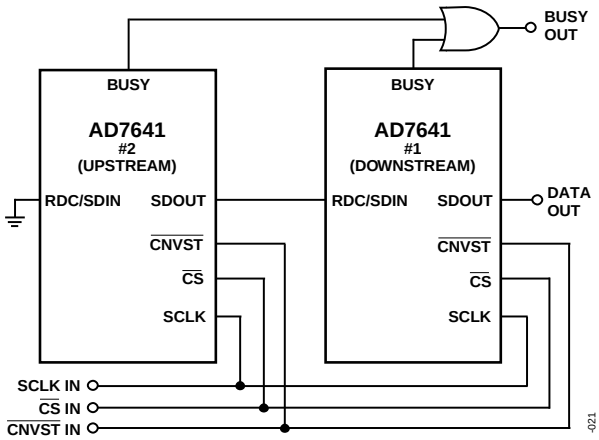


Figure 41.Two AD7621s in a Daisy-Chain Configuration

External Clock Data Read (Previous) During Conversion

Figure 43 shows the detailed timing diagrams of this method. During a conversion, while both $\overline{CS}$ and $\overline{RD}$ are both low, the result of the previous conversion can be read. The data is shifted out, MSB first, with 18 clock pulses and is valid on both rising and falling edge of the clock. The 18 bits have to be read before the current conversion is complete, otherwise, RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading. There is no "daisy chain" feature in this mode and RDC/SDIN input should always be tied either high or low.

To reduce performance degradation due to digital activity, a fast discontinuous clock (at least 30MHz when Impulse mode is used, 60 MHz when Normal mode is used, or 80 MHz when Warp mode is used) is recommended to ensure that all the bits are read during the first half of the SAR conversion phase.

It is also possible to begin to read data after conversion and continue to read the last bits after a new conversion has been initiated. However, this is not recommended if using the fastest throughput of any mode since the acquisition times are only 100ns and 147ns Warp and Normal modes.

If the maximum throughput is not used, thus allowing more acquisition time, then the use of a slower clock speed can be used to read the data.

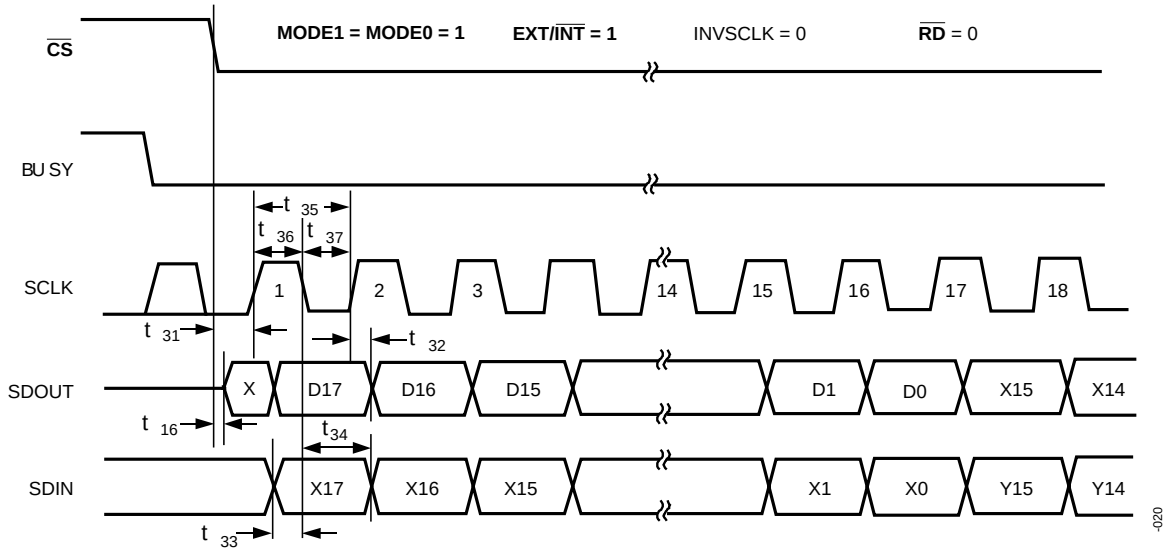


Figure 42. Slave Serial Data Timing for Reading (Read After Convert)

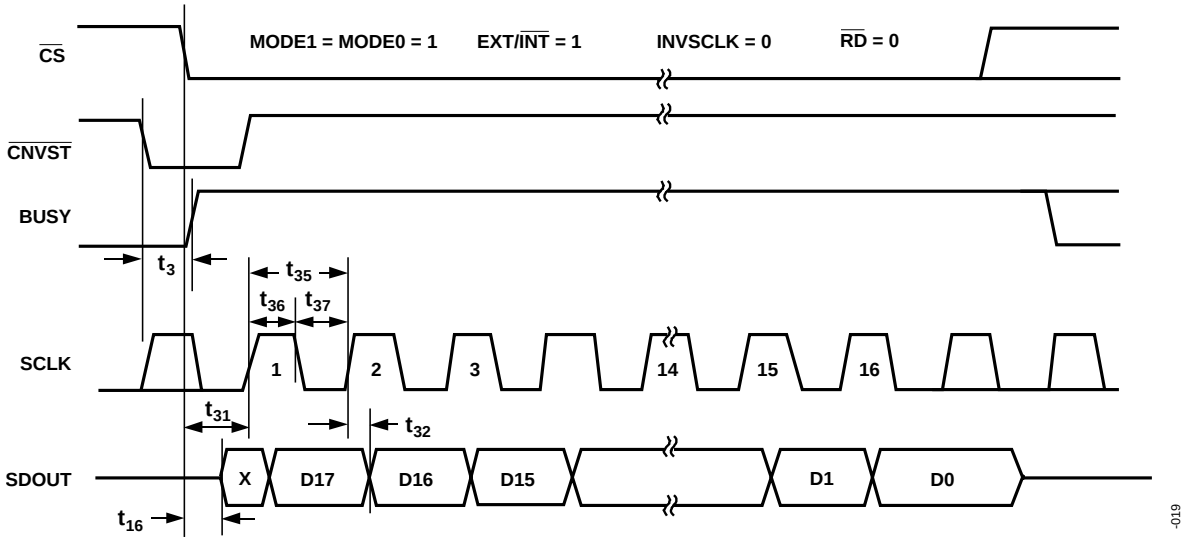


Figure 43. Slave Serial Data Timing for Reading (Read Previous Conversion During Convert)

MICROPROCESSOR INTERFACING

The AD7641 is ideally suited for traditional dc measurement applications supporting a microprocessor, and ac signal processing applications interfacing to a digital signal processor. The AD7641 is designed to interface either with a parallel 8-bit or 16-bit wide interface or with a general purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7641 to prevent digital noise from coupling into the ADC. The following section illustrates the use of the AD7641 with an SPI equipped DSP, the ADSP-219x.

SPI Interface (ADSP-219x)

Figure 43 shows an interface diagram between the AD7641 and an SPI-equipped DSP, ADSP219x. To accommodate the slower speed of the DSP, the AD7641 acts as a slave device and data must be read after conversion. This mode also allows the "daisy chain" feature. The convert command could be initiated in response to an internal timer interrupt. The 18-bit output data are read with 3 SPI byte access. The reading process could be initiated in response to the end-of-conversion signal (BUSY going low) using an interrupt line of the DSP. The Serial Peripheral Interface (SPI) on the ADSP-219x is configured for master mode (MSTR) = 1, Clock Polarity Bit (CPOL) = 0, Clock Phase Bit (CPHA) = 1 and SPI interrupt enable (TIMOD) =00 by writing to the SPI Control Register (SPICLTx). It should be noted that to meet all timing requirements, the SPI clock should be limited to 17Mbits/s which allow to read an ADC result in about 1.1 µs. When higher sampling rate is desired, it is recommended to use one of the parallel interface mode with the ADSP-219x.

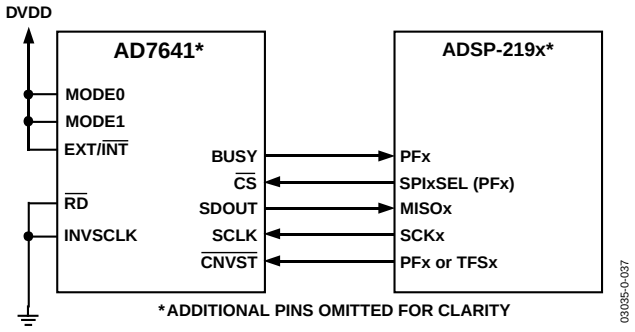


Figure 44. Interfacing the AD7641 to SPI Interface

APPLICATION HINTS

LAYOUT

The AD7641 has very good immunity to noise on the power supplies. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD7641 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7641, or, at least, as close as possible to the AD7641. If the AD7641 is in a system where multiple devices require analog to digital ground connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD7641.

It is recommended to avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7641 to avoid noise coupling. Fast switching signals like $\overline{\text{CNVST}}$ or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This will reduce the effect of feedthrough through the board. The power supply lines to the AD7641 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the supplies impedance presented to the AD7641 and reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on each power supplies pins AVDD, DVDD and OVDD close to, and ideally right up against these pins and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The DVDD supply of the AD7641 can be either a separate supply or come from the analog supply, AVDD, or from the digital interface supply, OVDD. When the system digital supply is noisy, or fast switching digital signals are present, it is recommended if no separate supply is available, to connect the DVDD digital supply to the analog supply AVDD through an RC filter as shown in Figure 26, and connect the system supply to the interface digital supply OVDD and the remaining digital circuitry. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high-frequency spikes.

The AD7641 has four different ground pins; REFGND, AGND, DGND, and OGND. REFGND senses the reference voltage and should be a low impedance return to the reference because it carries pulsed currents. AGND is the ground to which most internal ADC analog signals are referenced. This ground must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depending on the configuration. OGND is connected to the digital system ground.

The layout of the decoupling of the reference voltage is important. The decoupling capacitor should be close to the ADC and connected with short and large traces to minimize parasitic inductances.

EVALUATING THE AD7641 PERFORMANCE

A recommended layout for the AD7641 is outlined in the documentation of the EVAL-AD7641-CB, evaluation board for the AD7641. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the Eval-Control BRD3.

OUTLINE DIMENSIONS

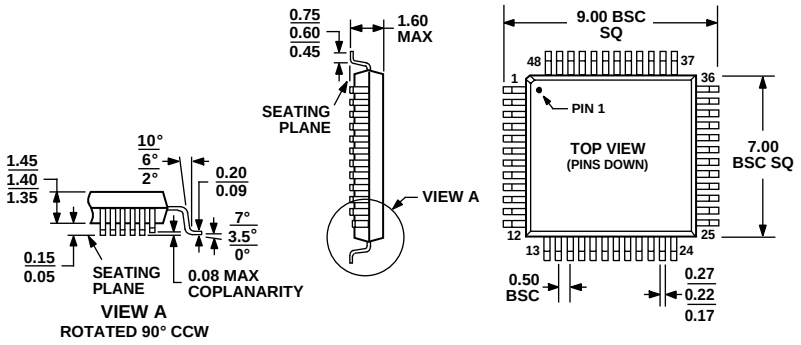


Figure 45. 48-Lead Quad Flatpack (LQFP) [ST-48]
Dimensions shown in millimeters

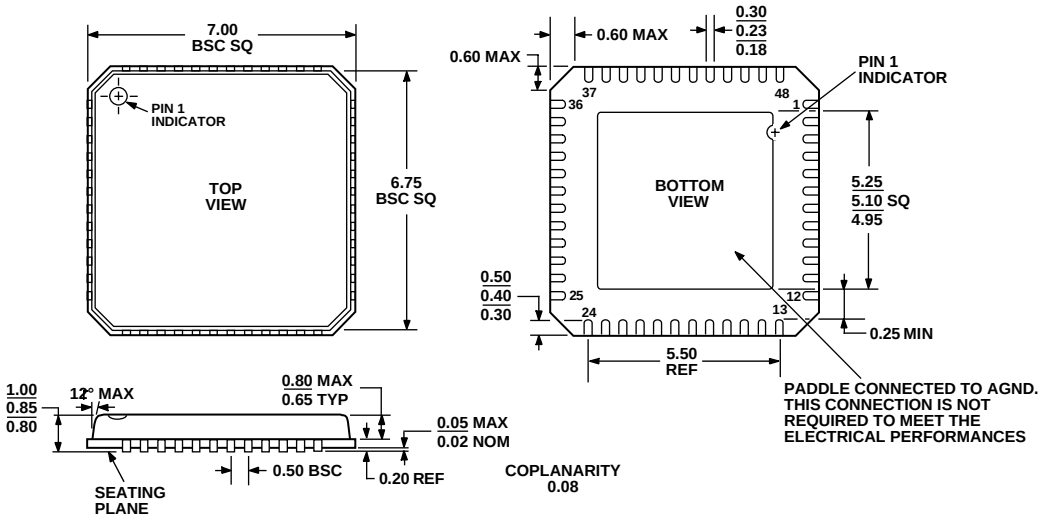


Figure 46. 48-Lead Frame Chip Scale Package (LFCSP) [CP-48]
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7641AST	-40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7641ASTRL	-40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7641ACP	-40°C to +85°C	Chip Scale (LFCSP)	CP-48
AD7641ACPRL	-40°C to +85°C	Chip Scale (LFCSP)	CP-48
EVAL-AD7641CB[1]		Evaluation Board	
EVAL-CONTROL BRD2[2]		Controller Board	
EVAL-CONTROL BRD3[2]		Controller Board	

[1] This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRD3 for evaluation/demonstration purposes.
[2] This board allows a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

PR04761–0–3/05(PrF)

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